AMENDMENTS TO THE DRAWINGS:

The drawings are amended as described below by presenting replacement figures as attached hereto.

Fig. 2 has been amended including a location determining unit, an external processing unit in the location determining unit, and a fuse blowing unit. The location determining unit and the fuse blowing unit are coupled to a BSIT 106, in accordance with the description provided in the Specification and recitations of the claims.

REMARKS

The Office Action dated November 18, 2004 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

In accordance with the foregoing, claims 2 and 13 have been amended to improve clarity of the features recited therein. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-31 stand rejected and pending and under consideration.

OBJECTIONS TO THE DRAWINGS:

In the Office Action, at page 2, the drawings were objected to. In view of the accompanying Replacement Sheets, corrections to Fig. 2 have been done. Therefore, the outstanding drawing objections should be resolved.

Reconsideration and withdrawal of the outstanding objections to the drawings are respectfully requested.

OBJECTIONS TO THE CLAIMS:

In the Office Action, at page 2, claim 2 was objected to. Claim 2 has been amended to correct a minor informality. Accordingly, it is respectfully requested that the objection to the claim be withdrawn.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 3, claims 1-5, 7-24, and 26-31 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,574,763 to Bertin et al. ("Bertin"). The Office Action took the position that Bertin discloses all the aspects of dependent claims 1-5, 7-24, and 26-31. The rejection is traversed and reconsideration is requested.

Independent claim 1, upon which claims 2-12 are dependent, recites a network device includes a buffer memory having a plurality of memory locations including redundant memory locations, the memory locations having addresses, a plurality of network ports, and a memory controller coupled to the buffer memory and configured to read and write data from and to the buffer memory. A first plurality of fuses in the network device is coupled to the redundant memory locations of the buffer memory and a second plurality of fuses is coupled to the memory controller and configured to store an address of a failed memory location of the plurality of memory locations. A built-in self test unit in the network device is coupled to the buffer memory and to the second plurality of fuses, and configured to perform a test of the buffer memory to determine an address of a failed memory location of the plurality of memory locations, and to store the address of the failed memory location in a fuse of the second plurality of fuses. The memory controller is configured to prevent a use of the failed memory location based on the address stored in the fuse.

Independent claim 13, upon which claims 14-19 are dependent, recites a method for testing buffer memory coupled to a memory controller and a flow controller, the method comprising the steps of: testing the buffer memory having a plurality of memory locations including redundant memory locations, to determine if any of the plurality of memory locations are unusable, determining an address of a first unusable memory location of the plurality of memory locations, and storing the address of the first unusable memory location, preventing a use of the first unusable memory location based on the stored address of the unusable memory location. The method further couples the flow controller to a plurality of network ports and to the memory controller, requests buffer pointers based on a data packet received at a network port of the plurality of network ports, and provides the buffer pointers to the flow controller without using the first unusable memory location based on the address stored in the unusable memory location.

Independent claim 20, upon which claims 21-31 are dependent, recites a network device includes a buffer memory means having a plurality of memory locations including redundant memory locations, the memory locations having addresses, a plurality of network ports, and a memory controller means coupled to the buffer memory and for reading and writing data from and to the buffer memory means. A first plurality of fuse means in the network device is coupled to the redundant memory locations of the buffer memory means and a second plurality of fuse means is coupled to the memory controller and for storing an address of a failed memory location of the plurality of memory locations. A built-in self test means in the network device is coupled to the buffer

memory means and to the second plurality of fuse means, for performing a test of the buffer memory means to determine an address of a failed memory location of the plurality of memory locations, and for storing the address of the failed memory location in a fuse means of the second plurality of fuse means. The memory controller means is for preventing a use of the failed memory location based on the address stored in the fuse means.

As will be discussed below, the cited reference of Bertin fails to disclose or suggest the elements of any of the presently pending claims.

Bertin generally describes a test circuit for generating a test pattern and for applying the test pattern to the memory array 103 so as to test all bits within a memory array 103. See column 2, lines 15-17. A comparison circuit, coupled to the test circuit and adapted to couple to the memory array, compares an actual response and an expected response of the memory array 103 to the test pattern and detects faulty and operable bits based thereon. See column 2, lines 17-21. A failed address buffer register, coupled to the comparison circuit and to the test circuit, stores an address of each addressable storage location that has a faulty bit. See column 6, lines 28-30. A data comparison circuit 403 compares the actual response of each bit within the memory array 103 to the applied test pattern and the expected response of the memory array 103 to the applied test pattern, and detects faulty and operable bits based thereon.

A failed address buffer register 405 coupled to the data comparison circuit 403 and to the test control circuit 401, and sparing control logic 407 coupled to the memory array

103 and to the failed address buffer register 405. See column 5, lines 24-28. The failed address buffer register 405 stores the address of each address location having at least one faulty bit. See column 7, lines 28-42. After the testing is complete (e.g., after a stop command is issued by the controller 107), a repair mode in Bertin is invoked and a sparing control logic 407 receives each address stored by the failed address buffer register 405 and decodes each failed address to a binary stream.

However, Bertin is silent as to teaching or suggesting, "a first plurality of fuses coupled to said redundant memory locations of said buffer memory," as recited in independent claim 1. Rather, as shown in Fig. 4 and corresponding description, the failed address buffer register 405 is coupled to the data comparison circuit 403 and to sparing control logic 407. As can also be appreciated from Fig. 4 of Bertin, the failed address buffer register 405 is not coupled to the memory array 103, which, according to the Office Action, corresponds to the buffer memory recited in independent claim 1.

Furthermore, contrary to the contentions made in the Office Action, Bertin merely provides that the data comparison circuit 403 compares the actual response of each bit within the memory array 103 to the applied test pattern and the expected response of the memory array 103 to the applied test pattern, and detects faulty and operable bits based thereon. See column 7, lines 28-34. In response thereto, the failed address buffer register 405 of Bertin stores the address of each address location having at least one faulty bit. However, Bertin is silent as to teaching or suggesting, "a second plurality of fuses coupled to said memory controller and configured to store an address of a failed memory

location of said plurality of memory locations," as recited in independent claim 1. There is no teaching or suggestion of coupling a second plurality of fuses to the test control circuit 401. Further, Bertin is silent as to teaching or suggesting, "a built-in self test unit coupled to said buffer memory and to said second plurality of fuses," as recited in independent claim 1. Instead, the data comparison unit 403 is coupled to the failed address buffer register 405 and the test control circuit 401, which, according to the Office Action, corresponds to the memory controller recited independent claim 1.

In addition, after the testing is complete in Bertin, a repair mode is invoked and the sparing control logic 407 receives each address stored by the failed address buffer register 405 and decodes each failed address to a binary stream which correlates to a fuse string required to activate redundant element address steering (e.g., which fuses/antifuses must be blown/unblown to activate the appropriate address redundancy for redundancy replacement). See column 7, lines 35-43. The sparing control logic 407 also energizes the high voltage generators required to activate the appropriate fuse strings and/or antifuse strings and thereby enable the redundant elements to replace the failed bit in the memory array 103. Thus, rather than teaching or suggesting "wherein said memory controller is configured to prevent a use of said failed memory location based on said address stored in said fuse," as recited in independent claim 1, Bertin provides that the fuse and/or antifuse strings are activated to replace the failed bit in the memory 103 to log array defects during elevated temperature testing/burn-in processes and subsequently be corrected at lower temperatures.

Bertin does not provide that the data comparison circuit 403 stores said address of said failed memory location "in a fuse of said second plurality of fuses" as recited in independent claim 1. Instead, Bertin provides that the data comparison circuit 403 compares the actual response of each bit within the memory array 103 and the expected response of the memory array 103 and the failed address register 405 stores the address for redundancy replacement.

By merely describing that the fuses/antifuses must be blown/unblown to activate the appropriate address redundancy for redundancy replacement, such description does not teach or suggest the recitations of the first plurality of fuses, the second plurality of fuses, and configuration of the memory controller of independent claim 1.

On page 3 of the Office Action, it is acknowledged that Bertin fails to teach or suggest the recitations of the second plurality of fuses or fuse means as recited in independent claims 1 and 20. Thus, it is contended that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to realize that his failed address buffer register performs equivalent function to that of second plurality of fuses, since it store the address of each memory location having faulty bits, and furthermore, he also teaches as stated above address steering and fuses/antifuses must be blown to activate the appropriate address redundancy, thus provides motivation for a person of ordinary skill in the art to utilize fuses to store an address of a failed memory location." However, as previously argued, the structural and functional recitations of the first plurality of fuses, the second plurality of fuses, and the memory controller of the

presently claimed application are distinct from the data comparison circuit 403, the failed address buffer register 405, and the test control circuit 401 of Bertin.

It is improper to merely deem something obvious without any teaching/suggestion, or the taking of Official Notice. "It is fundamental that rejections under 35 U.S.C. §103 must be based on evidence comprehended by the language of that section." See In re Lee 61 USPQ2d 1430 (CA FC 2002) (citing In re Grasselli, 713 F.2d 731, 739, 218 USPQ 769, 775).

If the U.S. Patent and Trademark Office wishes to take Official Notice that "a second plurality of fuses coupled to said memory controller and configured to store an address of a failed memory location of said plurality of memory locations...and to store said address of said failed memory location in a fuse of said second plurality of fuses...," is notoriously well known, Applicant respectfully requests to the U.S. Patent and Trademark Office that supporting evidence be provided. The Federal Circuit has cautioned that an Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. In re Rouffet, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998).

While "official notice" may be relied upon, as noted in MPEP §2144.03, these circumstances should be rare when an application is under final rejection or action under 37 CFR §1.113. According to MPEP 2144.03, "the examiner may take official notice of facts outside of the record which are capable of instant and unquestionable demonstration

as being 'well-known' in the art," emphasis added. However, if the Applicant, according to MPEP 2144.03 traverses such an assertion the examiner should cite a reference in support of his or her position. In short, the rules of the U.S. Patent and Trademark Office do not allow discretion on the part of the Examiner. Accordingly, the Applicant respectfully traverses such rejection and requests that either the Examiner must support his assertion with an Affidavit or withdraw the rejection.

The outstanding rejection would appear to have taken the teachings of the present invention and applied the same to modify Bertin, as set forth in the Office Action, to then disclose the presently claimed invention. Applicant respectfully asserts that the prima facie burden has not been met.

Because independent claim 20 includes similar claim features as those recited in independent claim 1, although of different scope, and because the Office Action refers to similar portions of the cited references to reject independent claim 20, the arguments presented above supporting the patentability of independent claim 1 are incorporated herein to support the patentability of independent claim 20.

Referring to independent claim 13, this claim recites, "requesting buffer pointers based on a data packet received at a network port of said plurality of network ports; and providing the buffer pointers to said flow controller without using said first unusable memory location based on the address stored in said unusable memory location." Bertin completely lacks any teaching or suggestion that the method described therein requests and provides buffer pointers "without using said first unusable memory location based on

the address stored in said unusable memory location," as recited in independent claim 13. Thus, it is respectfully asserted that in view of the description provided in Bertin, a person of ordinary skill in the art would not have arrived to the recitations of the presently claimed application.

In view of the foregoing, it is respectfully requested that independent claims 1, 13, and 20 and related dependent claims be allowed.

In the Office Action, at page 5, claims 6 and 25 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,574,763 to Bertin et al. ("Bertin") in view U.S application No. 2002/0169922 to Thomann et al. ("Thomann"). The Office Action took the position that Bertin and Thomann disclose all the aspects of dependent claims 6 and 25. The rejection is traversed and reconsideration is requested.

Dependent claim 6 depends from independent claim 1 and recites the additional features of "a flow controller coupled to said plurality of network ports and to said memory controller, and configured to request buffer pointers based on a data packet received at a network ports of said plurality of network ports; wherein, said memory controller is configured to provide buffer pointers to said flow controller without using any failed memory locations based on data stored in said second plurality of fuses." Further, dependent claim 25 depends from independent claim 20 and recites the additional features of "a flow controller coupled to said plurality of network ports and to said memory controller, and configured to request buffer pointers based on a data packet received at a network ports of said plurality of network ports; wherein, said memory

controller is configured to provide buffer pointers to said flow controller without using any failed memory locations based on data stored in said second plurality of fuses." Because the combination of Bertin and Thomann must teach, individually or combined, all the recitations of the base claim and any intervening claims of dependent claims 6 and 25, the arguments presented above supporting the patentability of independent claims 1 and 20 over Bertin are incorporated herein.

As will be discussed below, the cited references of Bertin and Thomann fail to disclose or suggest the elements of any of the presently pending claims.

Thomann generally provides a read/write timing calibration of a memory array using a row or a redundant row. In particular, Thomann provides that during operation of a memory device 100, if an address pad 120 and a fuse bank 124 receive a memory address including a row address (or, optionally, a column address) corresponding to a row address stored in the fuse bank 124, the fuse bank 124 sends a match signal to the address decoder 128 directing the address decoder 128 to select a redundant row 114 (or, optionally, a redundant column) rather than the row 112 including the failed memory cell 111. See page 6, column 1, lines 8-10.

However, Thomann does not cure the deficiencies of Bertin. For instance, similarly to Bertin, Thomann is devoid of any description or suggestion of providing, at least, "a first plurality of fuses coupled to said redundant memory locations of said buffer memory; a second plurality of fuses coupled to said memory controller and configured to store an address of a failed memory location of said plurality of memory locations."

Thomann does not even broach the concept of configuring a memory controller to prevent a use of a failed memory location based on an address stored in a fuse of the second plurality of the fuses as in the present invention. Thus, even if Bertin and Thomann were combined, a combination thereof would not provide for all the recitations of independent claim 1 and independent claim 20.

In view of the foregoing, it is respectfully requested that independent claims 1 and 20 and related dependent claims be allowed.

CONCLUSION:

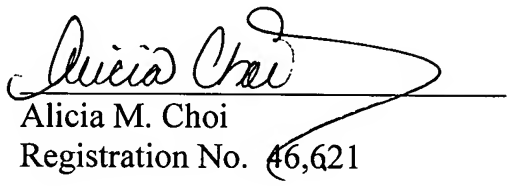
In view of the above, applicant respectfully submits that the claimed invention recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicant further submits that the subject matter is more than sufficient to render the claimed invention unobvious to a person of skill in the art. Applicant therefore respectfully requests that each of claims 1-31 and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time.

Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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Enclosures: Replacement Sheet Fig. 2